A CASCADED-IMPEDANCE-INVERTER MODEL OF WIDE-BAND FREQUENCY TRIPLERS*

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Summary

A charge-storage diode frequency tripler can be modeled as two cascaded impedance inverters. This approach has been used to design and construct a tripler at 1.06 GHz input frequency with a measured midband efficiency of 50% and a 3 dB bandwidth of 38%.

It has been demonstrated recently[1] that it is possible to design and construct broadband frequency triplers of high efficiency using charge-storage diodes (experimentally 45% bandwidth, 70% midband efficiency at 100-MHz input frequency). The design procedure used is based on a computer analysis similar to that used by Burkhardt.[2] This method is an effective one; however, extensive computer time is required to complete a design. An alternative approach is to model the diode behavior by a cascade of two impedance inverters. While this approach is exact only under one set of operating conditions which can occur only at a single frequency, it is a much simpler approach which has been found to give results, over a wide range of frequencies, which are not greatly different from those obtained from the more involved computer analysis. (This approach is similar to the one recently developed for the design of wide-band doublers.[3])

The basic tripler model used incorporates an ideal charge-storage diode with current flow allowed at the input frequency, output frequency, and second harmonic idler frequency.

The voltage-charge relationship for an ideal charge-storage diode is given by:

$$V(q) = qS_{max} \qquad q>0$$
$$= 0 \qquad q\leq 0$$

where S_{max} is the elastance of the reversed-biased diode. A constant resistance R_s is assumed to be in series with this piecewise linear elastance. The charge stored in the diode may be represented by:

$$q = q_o+q_1\cos(\omega t)+q_2\cos(2\omega t+\theta_2) +q_3\cos(3\omega t+\theta_3) .$$

Using the computer, the optimum efficiency for a given q_o, q_1, θ_2, θ_3 and diode Q (Q defined as $S_{max}/R_s\omega$) can be found. It has been useful to plot this data as a contour plot of efficiency as a function of θ_2 and θ_3. Such a contour plot is shown in Fig. 1 for $q_o = 0$ and a diode Q = 40. Note that efficiency is high along a straight line through the point $\theta_2 = \pi/2$, $\theta_3 = 0$, with unity slope. (The center point along this high-efficiency "ridge", $\theta_2 = \pi/2$, $\theta_3 = 0$, is the point used by Steinbrecher.[4]) Each point on the contour plot corresponds to a particular impedance at the first, second, and third harmonics. Wide-band operation can be achieved with no degradation in efficiency if multiplier network impedances can be synthesized which vary with frequency along the high-efficiency region of the contour plot.

The complete computer analysis shows that the optimum diode input and load resistances change rapidly in the neighborhood of $\theta_2 = \pi/2$, $\theta_3 = 0$. Since abrupt changes in impedance levels are at best difficult to synthesize, the contour plot center point should occur near the end of the frequency range of operation. This is accomplished by resonating the idler circuit at the high end of the band rather than at midband.

The ideal diode model reduces exactly to the impedance inverter structure in Fig. 2 at the ridge central point. The parameters in this circuit model are defined as:

$$K_1 = \frac{2}{3\pi}\frac{S_{max}}{\omega} \qquad K_2 = \frac{2}{5\pi}\frac{S_{max}}{\omega}$$

R_s = series resistance of diode.

$$C_o = \frac{2}{S_{max}}$$

Z_1 = 1*st* harmonic circuit impedance.

Z_2 = 2*nd* harmonic circuit impedance.

Z_3 = 3*rd* harmonic circuit impedance.

When the tripler operation departs from the ridge center point, the impedance inverter model is no longer an exact description. However, it has been empirically found to agree quite well with the exact approach when the tripler is operating in

the high-efficiency regions of the contour plot. Therefore, the impedance inverter model is useful in predicting the frequency response of wide-band triplers which utilize a second harmonic idler circuit.

Using the impedance inverter model, a wide-band tripler was designed and constructed for operation at an input center frequency of 1.06 GHz. A balanced circuit was used to suppress the even harmonics and facilitate tuning of the second harmonic idler circuit. A circuit diagram of the tripler is shown in Fig. 3. Lumped elements C_1, L_2, C_3 and L_4, which form a simple low-pass filter, are simulated by 10Ω and 100Ω transmission lines that are short compared to a wavelength at the input frequency. The inductors L_5 are used to tune the second harmonic resonance. Transmission lines Z_{01} and Z_{02} are a quarter wavelength at the output frequency and form a two-section bandpass filter. A two-section, quarter-wavelength transformer is employed at the output so that the proper value of R_L is obtained. The bias voltage is supplied by a low-impedance source.

The approximate circuit values used in the experimental tripler are:

C_1 = 3.2 pF C_3 = 5.0 pF
L_2 = 5.8 nH L_4 = 3.0 nH
R_L = 20Ω R_g = 50Ω
L_5 = 5.0 nH
Z_{01} = 80Ω, λ/4 at 4.2 GHz
Z_{02} = 50Ω, λ/4 at 3.3 GHz

The diodes used were a matched pair of MA4748 diodes. The total capacitance of each diode was approximately 0.5 pF at -10v bias.

The performance predicted by the impedance inverter model is sensitive to small changes in the value of the time-average capacitance of the diode. Therefore, care must be taken to accurately determine the operating capacitance of the diode. For the capacitance of the diodes used in this tripler, the parasitic package elements introduced some uncertainty into the time-average value to be used. A value of C_o = 0.9 pF was chosen as a reasonable value. The impedance inverter parameters calculated from this value of C_o are K_1 = 71Ω and K_2 = 43Ω. The series resistance R_s was determined empirically to be 8 ohms by matching the experimental and theoretical midband efficiency. Figure 4 is a plot of the measured efficiency versus frequency for this tripler with an input power of 300 mW and a bias voltage of 7 volts. The multiplier has a midband efficiency of approximately 50% and an instantaneous bandwidth of 38%. The graph shows both the experimental data and a curve based on the impedance inverter model. The agreement is considered good.

The second and fourth harmonic power output is down approximately 20 dB from the input signal. The fundamental power output is down 20 dB at the low end of the band, but it increases to approximately 12 dB down from the input power at the high end of the band.

In summary, a cascaded-impedance-inverter model of a charge-storage diode frequency tripler has been developed, and has been shown to be in agreement with the more exact model in predicting the frequency characteristics of a wide-band tripler. This circuit model should prove useful in the design of frequency triplers with bandwidths up to 50%, the bandwidth limitation on a balanced tripler because of harmonic interference.

References

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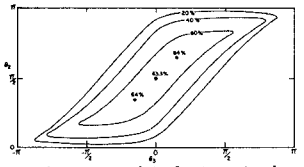

Fig. 1 Contour plot of optimum tripler efficiency as a function of phase angles θ_2 and θ_3, for q_o = 0 and Q = 40. For clarity, the complete plot is not shown; efficiency is periodic in θ_2 and θ_3.

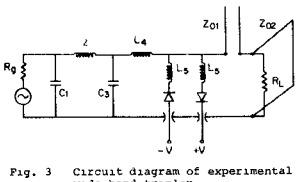

Fig. 3 Circuit diagram of experimental wide-band tripler.

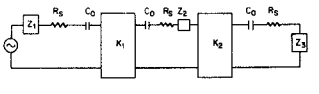

Fig. 2 Cascaded-impedance-inverter model of a frequency tripler with second harmonic idler circuit.

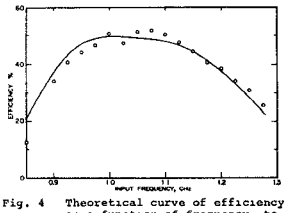

Fig. 4 Theoretical curve of efficiency as a function of frequency, together with experimental points.

Notes